

PROTOstic™

Embedded FPGA Controller Product Brief

PROTOstic™ is a small FPGA-based embedded computing product, designed for use as a flexible, customizable embedded controller. Additionally, PROTOstic™ can serve as a general purpose embedded FPGA co-processing element. PROTOstic™ is also designed to fit into two of the microcontroller slots in the rear of a RABA Core Foundry PROTEUS™ chassis.

The main features and capabilities of each PROTOstic™ include:

- Altera Cyclone FPGA, supporting 1C4/12/20 sized devices, any speed grade
 - Capable of running dual NIOS2 processors
 - Over 400 DMIPs of embedded processing power
 - Custom peripherals and instructions
 - uClinux supported
 - MicroC/OS-2 RTOS supported
 - Nucleus RTOS supported
- 10/100 ethernet connectivity
- SMSC LAN91C111 MAC+PHY chip (Directly supported by NIOS2)
- 16MB onboard FLASH
 - AMD 29LV128 family (Directly supported by NIOS2)
- SD/MMC socket supports up to 1GB memory
- Accepts WiFi and GPS SD cards
- Two independent PC100 compliant SDRAM chips
 - Board supports 8/16/32 MB x 32 bits wide for each chip
 - Micron MT48LC family (Directly supported by NIOS2)
- 54 GPIO pins connect FPGA to carrier board via standard 64-pin CMC connector
 - 32-bit PCI bus can be supported
- Mini USB AB connector supports USB 2.0 and OTG LS and FS speeds
 - Phillips ISP1362 host + peripheral controller
- Serial boot prom programming header
- Real Time Clock with onboard battery
- Two on-board oscillators
- JTAG header

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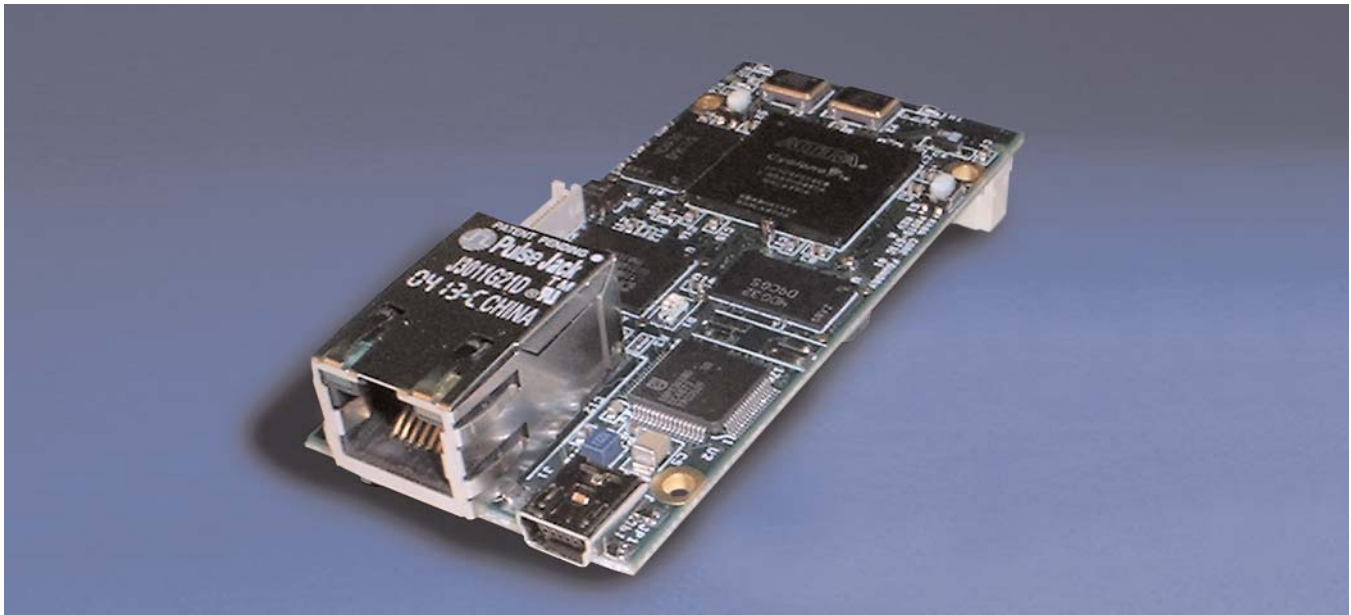
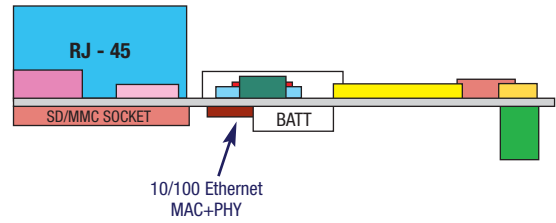
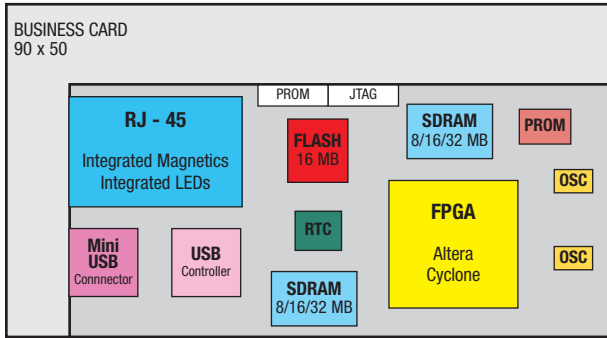
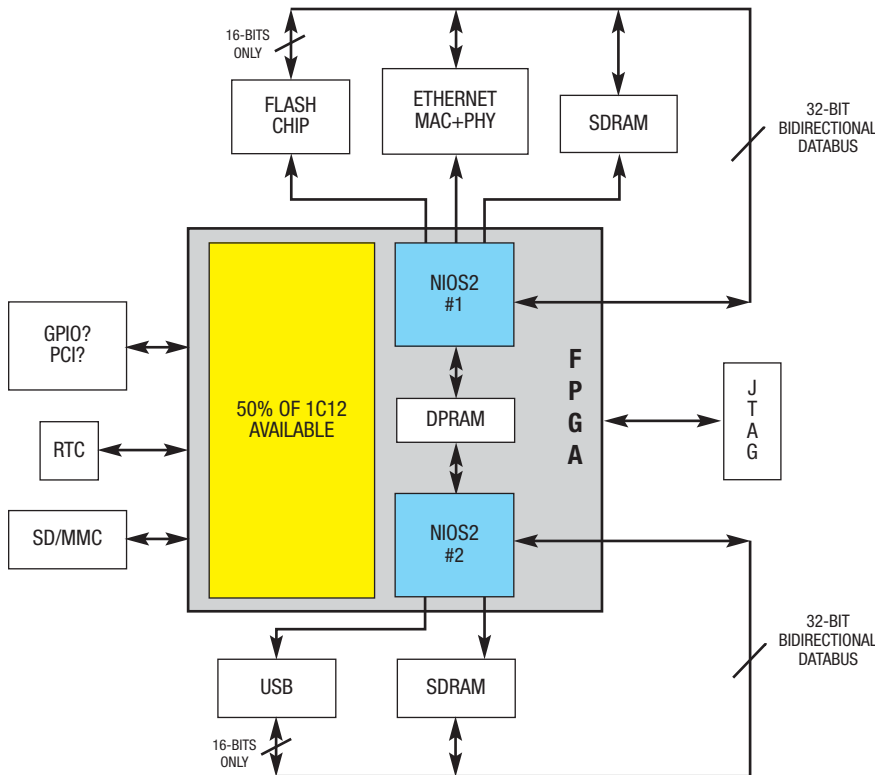


figure 1: PROTOstic™ Simple Block Diagram



Measuring only 38mm x 80mm, PROTOstic™ is smaller than a standard business card. Figure 1 shows a simple block diagram of the board.

figure 2: Peripheral Bus Structure



The use of two separate and independent SDRAMs allows PROTOstic™ to support two NIOS2 processors in the FPGA, each with its own SDRAM. One processor could run uClinux and service the 10/100 ethernet port, while a second processor could act as a process controller for the host board, and run an RTOS. A dual-port RAM could be used to allow the two processors to transfer data between them.

Or, a single processor could be instantiated with separate data and program memory. The various peripherals share data bus pins with one or the other SDRAM as shown in Figure 2.